#8/A

PTO/sb/ xx (6-95)
Approved for use through OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

0002/PTO

U.S. Department of Commerce
Patent and Trademark Office

FEE TRANSMITTAL

COMPLETE IF KNOWN	
Application Number	*To be assigned*
Filing Date	2 September 1997
First Named Inventor	Geun-Woo Park
Group Art Unit	*To be assigned*
Examiner Name	*To be assigned*
Attorney Docket Number	**P54766**

TOTAL AMOUNT OF PAYMENT	**$770.00**

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Account Number: **02-4943**
Deposit Account Name:

☒ Charge any additional fee required under 37 CFR 1.16 and 1.17

☐ Charge the issue Fee set in 37 CFR 1.18 at the mailing of the Notice of Allowance. 37 CFR 1.311 (b).

2. ☒ Payment enclosed:

☒ **Checks #21242**

☐ Money order

☐ Other

FEE CALCULATION

1. Filing FEE

Large Entity Fee Code	Large Entity Fee(s)	Small Entity Fee Code	Small Entity Fee(s)	Fee Description	Fee Paid
101	770	201	375	Utility filing	$ 770.00
106	310	206	155	Design filing fee	$
107	510	207	255	Plant filing Fee	$
106	750	206	375	Reissue filing fee	$
				SUBTOTAL (1)	$ 770.00

2. CLAIMS

Fee from below

Total Claims 7
independent claims: 2
Multiple Dependent claims:

Large Entity Fee Code	Large Entity Fee(s)	Small Entity Fee Code	Small Entity Fee(s)	Fee Description	Fee Paid
102	78	202	39	Independent claim In excess of three	$
103	22	203	11	Claim s in excess of 20	$
104	250	204	125	Multiple dependent claims	
109	78	209	39	Reissue independent claims over original patent	
110	22	210	11	Reissue claims in excess of 20 and over original patent	
				SUBTOTAL	$

ADDITIONAL FEES
Large Entity

submitted by: Robert E. Bushnell, Esq. (Payor No. 008-439) | Complete (is applicable)

Typed or Printed Name	Robert E. Bushnell			Reg. No.	27,774
Signature	R Bushnell	Date	September 2, 1997	Deposit Account User ID	

REB/kt

TITLE

DISPLAY DEVICE WITH POWER INTERRUPTION DELAY FUNCTION

CLAIM OF PRIORITY

This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C §119 from an application entitled *Display Apparatus With Power Interruption Delay Function* earlier filed in the Korean Industrial Property Office on 30 August 1996, and there duly assigned Serial No. 96-37143 by that Office.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates in general to a display device employing a cathode ray tube, and more particularly to a display device with a power interruption delay function, in which a power interruption delay charging circuit is provided to prevent a horizontal output transistor from being damaged due to an instantaneous surge current generated when power supply is resumed under the condition that a high voltage charged on a horizontal deflection coil and an S-correction capacitor is not sufficiently discharged after power interruption.

Description of the Prior Art

Generally, a horizontal deflection circuit is supplied with power from a power supply circuit and controlled in operation by a microcomputer. Such a horizontal deflection circuit is an essential component of a display device.

Generally, in a display device a power supply circuit is adapted to convert commercial alternating current (AC) input power into direct current (DC) power to supply desired voltages to the horizontal deflection circuit and a control unit incorporating a microcomputer. The microcomputer is adapted to control the operations of the horizontal deflection circuit and the power supply circuit. The horizontal deflection circuit is adapted to horizontally deflect electron beams emitted from a cathode ray tube. An exemplary horizontal deflection circuit may include a pulse width modulation (PWM) controller for generating a PWM signal under the control of the microcomputer, a current amplifier for amplifying current in response to the PWM signal from the PWM controller, a horizontal/vertical (H/V) processor for driving a horizontal driver under the control of the microcomputer, an H/V processor constant voltage circuit for supplying a constant voltage to the H/V processor to drive it, and a horizontal output circuit for supplying current to a horizontal deflection coil and an S-correction capacitor in response to output signals from the current amplifier and horizontal driver.

The operation of the horizontal deflection circuit of the exemplary display device with the above-mentioned construction will hereinafter be described.

When the display device is powered on, the PWM controller is operated under the control of the microcomputer to output the PWM signal to the current amplifier and a high voltage from the high voltage source is transferred to the horizontal deflection coil and the S-correction capacitor.

Under the above condition, the H/V processor outputs a horizontal pulse signal of square wave to the horizontal driver under the control of the microcomputer. As a result, the high voltage charged on the horizontal deflection coil and S-correction capacitor is discharged to a ground voltage terminal.

Thereafter, when the square wave pulse signal from the H/V processor is changed from high to low in level, and the high voltage from the horizontal deflection coil and S-correction capacitor is no longer discharged.

Then, the high voltage from the high voltage source is again transferred to the horizontal deflection coil and S-correction capacitor. Hence, the above-mentioned operation is repeated.

Noticeably, the horizontal deflection coil is mounted to a neck portion of a display device so that electron beams can be deflected to the left or right according to a direction of current flowing through the coil.

The S-correction capacitor applies a parabola voltage to the horizontal deflection coil to correct a linearity of center-to-left and right sides of a screen of the display device. The S-correction capacitor also performs a DC interruption function for preventing DC current from flowing to the horizontal deflection coil.

If the power supply to the display device is interrupted during the operation of the display device, the H/V processor constant voltage circuit operates no longer due to interruption of the voltage. As a result, the H/V processor operates no longer, as well.

As the H/V processor operates no longer, it outputs no pulse signal thereby causing the high voltage charged on the horizontal deflection coil and S-correction capacitor not to be discharged. As a result, a voltage of about +120 to 160 V remains.

Under the above condition, if the power supply to the display device is resumed, the H/V processor constant voltage circuit is driven because of application of a voltage so as to operate the H/V processor, a high voltage with a very high peak value (about +1.5 to 1.8KV) is instantaneously generated. As a result, a surge current resulting from the instantaneous high voltage abruptly flows through a discharge loop damaging a portion of the horizontal output circuit.

If the horizontal output circuit is damaged, no horizontal deflection is performed on the screen of the display device, thereby causing a single line to be vertically drawn on the center of the screen. As a result, the user cannot recognize the information displayed on the screen.

Further, the peripheral devices and circuits may successively be damaged due to a short-circuit resulting from the damage in the horizontal output circuit.

SUMMARY OF THE INVENTION

Therefore, the present invention has been made in view of the above problems, and it is an object of the present invention to provide a display device with a power interruption delay function, in which a power interruption delay charging circuit is provided to prevent a horizontal output transistor from being damaged due to an instantaneous surge current generated when power supply is resumed under the condition that a high voltage charged on a horizontal deflection coil and an S-correction capacitor is not sufficiently discharged after power interruption.

In accordance with the present invention, the above and other objects can be accomplished by a provision of a display device with a power interruption delay function, comprising a pulse width modulation controller for generating a pulse width modulation signal under the control of a microcomputer; a current amplifier for amplifying current in response to the pulse width modulation signal from the pulse width modulation controller; an H/V processor for generating a square wave pulse signal under the control of the microcomputer; a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from the H/V processor; a horizontal deflection coil for horizontally deflecting electron beams; an S-correction capacitor connected in series to the horizontal deflection coil, for correcting a linearity of center-to-left and right sides of a screen; a horizontal output circuit for charging and discharging energy on the horizontal deflection coil and S-correction capacitor in response to an output signal from the current amplifier and the drive pulse

signal from the horizontal driver; an H/V processor constant voltage circuit for supplying a constant voltage to the H/V processor; and power interruption delay charging means for gradually lowering an input voltage to the H/V processor constant voltage circuit when power supply to the display device is interrupted.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the present invention, and many of the attendant advantages thereof, will become readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

Fig. 1 is a schematic block diagram illustrating the construction of a horizontal deflection circuit of a display device;

Fig. 2 is a detailed circuit diagram of the horizontal deflection circuit of the display device in Fig. 1;

Fig. 3 is a detailed circuit diagram illustrating the construction of a display device with a power interruption delay function in accordance with the principles of the present invention;

Figs. 4a and 4b are waveform diagrams showing comparison between inputs to H/V processor constant voltage circuits in Figs. 2 and 3; and

Figs. 5a and 5b are waveform diagrams showing comparison between outputs of H/V processors in Figs. 2 and 3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a schematic block diagram illustrating the construction of a horizontal deflection circuit of a display device. In this drawing, the reference numeral 110 designates a microcomputer, 120 designates a power supply circuit and 130 designates a horizontal deflection circuit.

The power supply circuit 120 is adapted to convert commercial alternating current (AC) input power into direct current (DC) power to supply desired voltages to the horizontal deflection circuit 130 and the microcomputer 110.

The microcomputer 110 is adapted to control the operations of the horizontal deflection circuit 130 and power supply circuit 120.

The horizontal deflection circuit 130 is adapted to horizontally deflect electron beams emitted from a cathode ray tube.

The horizontal deflection circuit 130 includes a pulse width modulation (PWM) controller 135 for generating a PWM signal under the control of the microcomputer 110, a current amplifier 136 for amplifying current in response to the PWM signal from the PWM controller 135, an H/V processor 132 for driving a horizontal driver 133 under the control of the microcomputer 110, an H/V processor constant voltage circuit 131 for supplying a constant voltage to the H/V processor 132 to drive it, and a horizontal output circuit 134 for supplying current to a horizontal deflection coil H-DY and an S-correction capacitor Cs in response to output signals from the current amplifier 136 and horizontal driver 133.

Fig. 2 is a detailed circuit diagram of the horizontal deflection circuit 130 of the display device in Fig. 1. As shown in this drawing, the current amplifier 136 includes a current amplification transformer T1 having primary and secondary coils, and a field effect transistor FET1 having its gate terminal connected to the secondary coil of the current amplification transformer T1.

The primary coil of the current amplification transformer T1 has its one side connected to an output terminal of the PWM controller 135 through a capacitor and its other side connected to a ground voltage terminal. The field effect transistor FET1 also has its drain terminal connected to a high voltage source B+ and its source terminal connected in common to one side of the horizontal deflection coil H-DY and a collector terminal of a horizontal output transistor TR in the horizontal output circuit 134 through a pulse transformer PT. The other side of the horizontal deflection coil H-DY is connected to one side of the S-correction capacitor Cs, the other side of which is connected to the ground voltage terminal.

The H/V processor constant voltage circuit 131 has its input terminal connected to a voltage source V1 and its output terminal connected in common to an input terminal of the H/V processor 132 and one side of a capacitor, the other side of which is connected to the ground voltage terminal. The horizontal driver 133 includes a field effect transistor FET2 having its gate terminal connected to an output terminal of the H/V processor 132 and its source terminal connected to the ground voltage terminal, and a horizontal drive transformer T2 having primary and secondary coils. The primary coil of the horizontal drive transformer T2 has its one side connected to a voltage source V2 through a resistor and its other side connected to a drain terminal of the field effect transistor FET2. The secondary coil of the horizontal drive transformer T2 has its one side connected to a base terminal of the horizontal output transistor TR in the horizontal output circuit 134, the emitter terminal of which is connected to the ground voltage terminal, and its other side connected to the ground voltage terminal.

The operation of the horizontal deflection circuit 130 of the display device with the above-mentioned construction will hereinafter be described.

When the display device is powered on, the PWM controller 135 is operated under the control of the microcomputer 110 to output the PWM signal to the current amplifier 136. In the

current amplifier 136, the current amplification transformer T1 is excited in response to the PWM signal from the PWM controller 135 to drive the field effect transistor FET1 connected to the secondary coil thereof. As the field effect transistor FET1 is driven, a high voltage from the high voltage source B+ connected to the drain terminal of the transistor FET1 is transferred to the horizontal deflection coil H-DY and S-correction capacitor Cs through the pulse transformer PT to be charged thereon.

Under the above condition, the H/V processor 132 outputs a horizontal pulse signal of square wave to the horizontal driver 133 under the control of the microcomputer 110. In the horizontal driver 133, the field effect transistor FET2 is turned on when the square wave pulse signal from the H/V processor 132 is high in level, to excite the horizontal drive transformer T2. As a result, a voltage is induced in the secondary coil of the horizontal drive transformer T2, thereby causing the horizontal output transistor TR in the horizontal output circuit 134 to be turned on. As the horizontal output transistor TR is turned on, it discharges the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs to the ground voltage terminal therethrough.

Thereafter, when the square wave pulse signal from the H/V processor 132 is changed from high to low in level, the field effect transistor FET2 and the horizontal output transistor TR are successively turned off. As a result, the high voltage from the horizontal deflection coil H-DY and S-correction capacitor Cs is no longer discharged.

Then, the high voltage from the high voltage source B+ is again transferred to the horizontal deflection coil H-DY and S-correction capacitor Cs through the field effect transistor FET1 and pulse transformer PT in the current amplifier 136 to be charged thereon. Hence, the above-mentioned operation is repeated.

Noticeably, the horizontal deflection coil H-DY is mounted to a neck portion (not shown) of the display device so that electron beams emitted from the cathode ray tube can be deflected to the left or right according to a direction of current flowing through the coil H-DY.

The S-correction capacitor Cs applies a parabola voltage to the horizontal deflection coil H-DY to correct a linearity of center-to-left and right sides of a screen of the display device. The S-correction capacitor Cs also performs a DC interruption function for preventing DC current from flowing to the horizontal deflection coil H-DY.

If the power supply to the display device is interrupted during the operation of the display device, the H/V processor constant voltage circuit 131 operates no longer due to interruption of the voltage V1 as shown in Fig. 4a. As a result, the H/V processor 132 operates no longer, as well.

As the H/V processor 132 no longer operates, it outputs no pulse signal as shown in Fig. 5a, thereby causing the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs not to be discharged. As a result, a voltage of about +120 to 160V remains at a node A of the collector terminal of the horizontal output transistor TR.

Under the above condition, if the power supply to the display device is resumed, the H/V processor constant voltage circuit 131 is driven because of application of the voltage V1, so as to operate the H/V processor 132. As a result, the horizontal output transistor TR is operated.

At this time, a high voltage with a very high peak value (about +1.5 to 1.8KV) is instantaneously generated at the collector terminal of the horizontal output transistor TR. As a result, a surge current resulting from the instantaneous high voltage abruptly flows through a discharge loop including the horizontal output transistor TR, thereby causing the horizontal output transistor TR to be damaged.

If the horizontal output transistor TR in the horizontal output circuit 134 is damaged, no horizontal deflection is performed on the screen of the display device, thereby causing a single line

to be vertically drawn on the center of the screen. As a result, the user cannot recognize the information displayed on the screen.

Further, the peripheral devices and circuits may successively be damaged due to a short-circuit resulting from the damage in the horizontal output transistor TR.

Fig. 3 is a detailed circuit diagram illustrating the construction of a display device with a power interruption delay function in accordance with the present invention. The construction of this drawing is the same as that of Fig. 2, with the exception that a power interruption delay charging circuit 370 is provided according to the present invention. Therefore, like reference numerals designate like parts and a detailed description thereof will thus be omitted.

In the display device of Fig. 2, the voltage source V1 is connected directly to the input terminal of the H/V processor constant voltage circuit 131. However, in the display device of Fig. 3, the voltage source V1 is connected to the input terminal of the H/V processor constant voltage circuit 131 through the power interruption delay charging circuit 370.

The power interruption delay charging circuit 370 includes a reverse voltage prevention diode D1 having its anode connected to the voltage source V1 and its cathode connected to the input terminal of the H/V processor constant voltage circuit 131, and a polarity capacitor C1 having its positive pole connected to a connection point of the cathode of the reverse voltage prevention diode D1 and the input terminal of the H/V processor constant voltage circuit 131 and its negative pole connected to the ground voltage terminal.

The operation of the display device with the above-mentioned construction in accordance with the present invention will hereinafter be described in detail.

When the display device is powered on, the high voltage from the high voltage source B+ is charged on the horizontal deflection coil H-DY and S-correction capacitor Cs through the field effect transistor FET1 and pulse transformer PT in the current amplifier 136 and then discharged

through the discharge loop including the horizontal output transistor TR in the horizontal output circuit 134. Such charging and discharging operations are repeated as stated previously with reference to Fig. 2.

If the power supply to the display device is interrupted during the operation of the display device, the voltage supply to the H/V processor constant voltage circuit 131 is at once stopped in the display device of Fig. 2, as shown in Fig. 4a. However, according to the present invention, a voltage, charged on the polarity capacitor C1 during the power supply, is applied to the input terminal of the H/V processor constant voltage circuit 131, as shown in Fig. 4b, while it is discharged. As a result, the H/V processor constant voltage circuit 131 does not immediately stop the voltage supply to the H/V processor 132.

Noticeably, the reverse voltage prevention diode D1 is connected in series between the voltage source V1 and the H/V processor constant voltage circuit 131 to protect the power supply circuit by allowing the voltage charged on the polarity capacitor C1 not to be discharged to the voltage source V1 at the power interruption state.

Because the voltage charged on the polarity capacitor C1 is continuously applied to the H/V processor constant voltage circuit 131 until it is completely discharged, the voltage supply to the H/V processor 132 is not interrupted immediately. Therefore, the H/V processor 132 outputs the horizontal pulse signal continuously for a predetermined time period, as shown in Fig. 5b.

The continuous pulse output time of the H/V processor 132 is determined according to a discharge time of the polarity capacitor C1. As a result, the continuous pulse output time of the H/V processor 132 can be varied by adjusting the discharge time of the polarity capacitor C1.

While the output pulse from the H/V processor 132 maintains such a high voltage level as to continuously drive the field effect transistor FET2 in the horizontal driver 133, the horizontal drive transformer T2 continues to be excited to induce a voltage in its secondary coil, thereby

causing the horizontal output transistor TR in the horizontal output circuit 134 to remain at its driven state. Hence, the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs can be sufficiently discharged. Namely, the discharge time of the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs is sufficient.

As apparent from the above description, according to the present invention, the power interruption delay charging circuit is provided at the input terminal of the H/V processor constant voltage circuit in the display device. The power interruption delay charging circuit can prevent the horizontal output transistor from being damaged due to an instantaneous surge current when power supply is resumed after power interruption. Further, the power interruption delay charging circuit can prevent the peripheral devices and circuits from being successively damaged due to damage in the horizontal output transistor.

Although the preferred embodiments of the present invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

WHAT IS CLAIMED IS:

1. A display device with a power interruption delay function, comprising:

a pulse width modulation controller for generating a pulse width modulation signal under the control of a microcomputer;

a current amplifier for amplifying current in response to the pulse width modulation signal from said pulse width modulation controller;

a horizontal/vertical processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said horizontal/vertical processor;

a horizontal deflection coil for horizontally deflecting electron beams generated in said display device;

a S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver;

a horizontal/vertical processor constant voltage circuit for supplying a constant voltage to said horizontal/vertical processor in response to an input voltage; and

power interruption delay charging means for gradually lowering said input voltage to said horizontal/vertical processor constant voltage circuit when power supplied to said display device is interrupted.

2. The display device as set forth in claim 1, wherein said power interruption delay charging means includes:

a polarity capacitor for performing a charging operation when power is supplied to said display device and a discharging operation when the power supplied to said display device is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supplied to the display device is interrupted.

3. A display device with a power interruption delay function, comprising:

a power supply circuit for converting a received commercial alternating current power into a direct current input voltage;

a horizontal deflection circuit under the control of a microcomputer, receiving said direct current input voltage, for horizontally deflecting electron beams generated in said display device; and

power interruption delay charging means for gradually lowering said direct current input voltage received by said horizontal deflection circuit when said alternating current power supplied to said power supply circuit is interrupted, said power interruption delay charging means comprising:

a polarity capacitor for performing a charging operation when said alternating current power is supplied and a discharging operation when said alternating current power is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to said power supply circuit when said alternating current power is interrupted.

4. The display device as set forth in claim 3, wherein said horizontal deflection circuit comprises:

a pulse width modulation controller for generating a pulse width modulation signal under the control of said microcomputer;

a current amplifier for amplifying current in response to said pulse width modulation signal generated by said pulse width modulation controller;

a horizontal/vertical processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said horizontal/vertical processor;

a horizontal deflection coil for horizontally deflecting said electron beams;

a S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver; and

a horizontal/vertical processor constant voltage circuit for supplying a constant voltage to said horizontal/vertical processor in response to said direct current input voltage, said direct current input voltage being received through said power interruption delay charging means.

5. The display device as set forth in claim 4, wherein said current amplifier comprises:

a current amplification transformer having a primary coil and a secondary coil;

a field effect transistor having its gate terminal connected to one terminal of said secondary coil;

one terminal of said primary coil being connected to an output terminal of said pulse width modulation controller through a capacitor and another terminal of said primary coil being connected to said ground terminal;

said field effect transistor having a drain terminal connected to a high voltage source and a source terminal connected in common to a second terminal of said secondary coil and one side of a pulse transformer;

said pulse transformer having a second side connected to one side of said horizontal deflection coil;

a first diode connected between said source terminal and said drain terminal; and

a second diode connected between said second terminal of said secondary coil and said ground terminal.

6. The display device as set forth in claim 5, wherein said horizontal output circuit comprises a horizontal output transistor having a collector terminal connected in common to said second side of said pulse transformer and said one side of said horizontal deflection coil, an emitter terminal connected to said S-correction capacitor and said ground terminal, and a base terminal connected to an output terminal of said horizontal driver for receiving said drive pulse signal.

7. The display device as set forth in claim 6, wherein said horizontal driver comprises:

a second field effect transistor having a gate terminal connected to receive said square wave pulse signal from said horizontal/vertical processor, a source terminal connected to said ground terminal, and a drain terminal;

a horizontal drive transformer having a primary coil and a secondary coil, said primary coil having one terminal connected to a voltage source through a resistor and a second terminal connected to said drain terminal of said second field effect transistor; and

said secondary coil of said horizontal drive transformer having one side connected to said base terminal of said horizontal output transistor and a second side connected to said ground terminal.

ABSTRACT OF THE DISCLOSURE

A display device with a power interruption delay function, comprising a power interruption delay charging circuit for gradually lowering an input voltage to an horizontal/vertical processor constant voltage circuit when power supply to the display device is interrupted. According to the present invention, when power supply is resumed under the condition that a high voltage charged on a horizontal deflection coil and an S-correction capacitor is not sufficiently discharged after power interruption, the power interruption delay charging circuit can prevent a horizontal output transistor from being damaged due to an instantaneous surge current resulting from the high voltage being not discharged.

FIG. 1

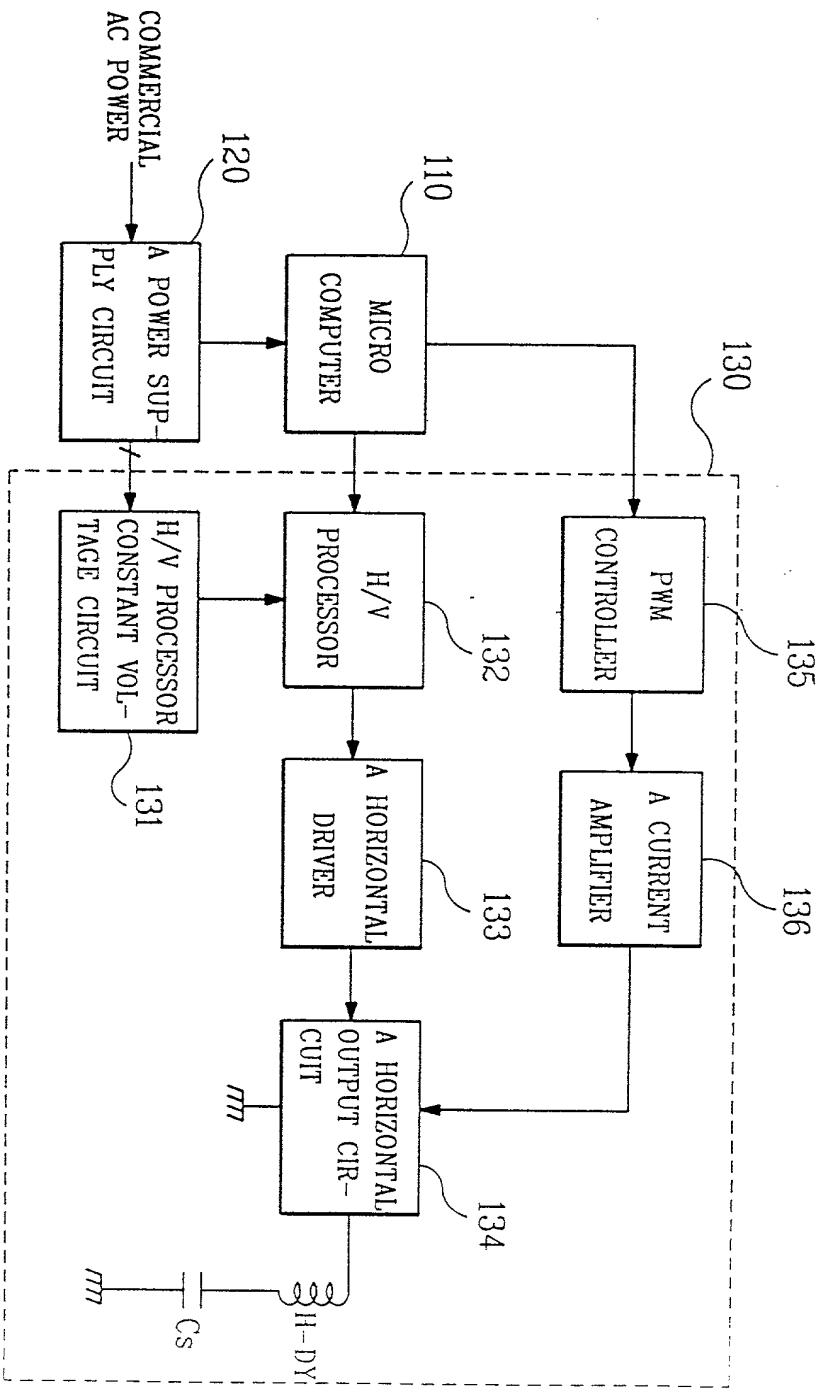

COMMERCIAL AC POWER
120
A POWER SUPPLY CIRCUIT
110
MICRO COMPUTER
130
PWM CONTROLLER
135
A CURRENT AMPLIFIER
136
H/V PROCESSOR
132
A HORIZONTAL DRIVER
133
A HORIZONTAL OUTPUT CIRCUIT
134
H/V PROCESSOR CONSTANT VOLTAGE CIRCUIT
131
Cs
H-DY

FIG. 2

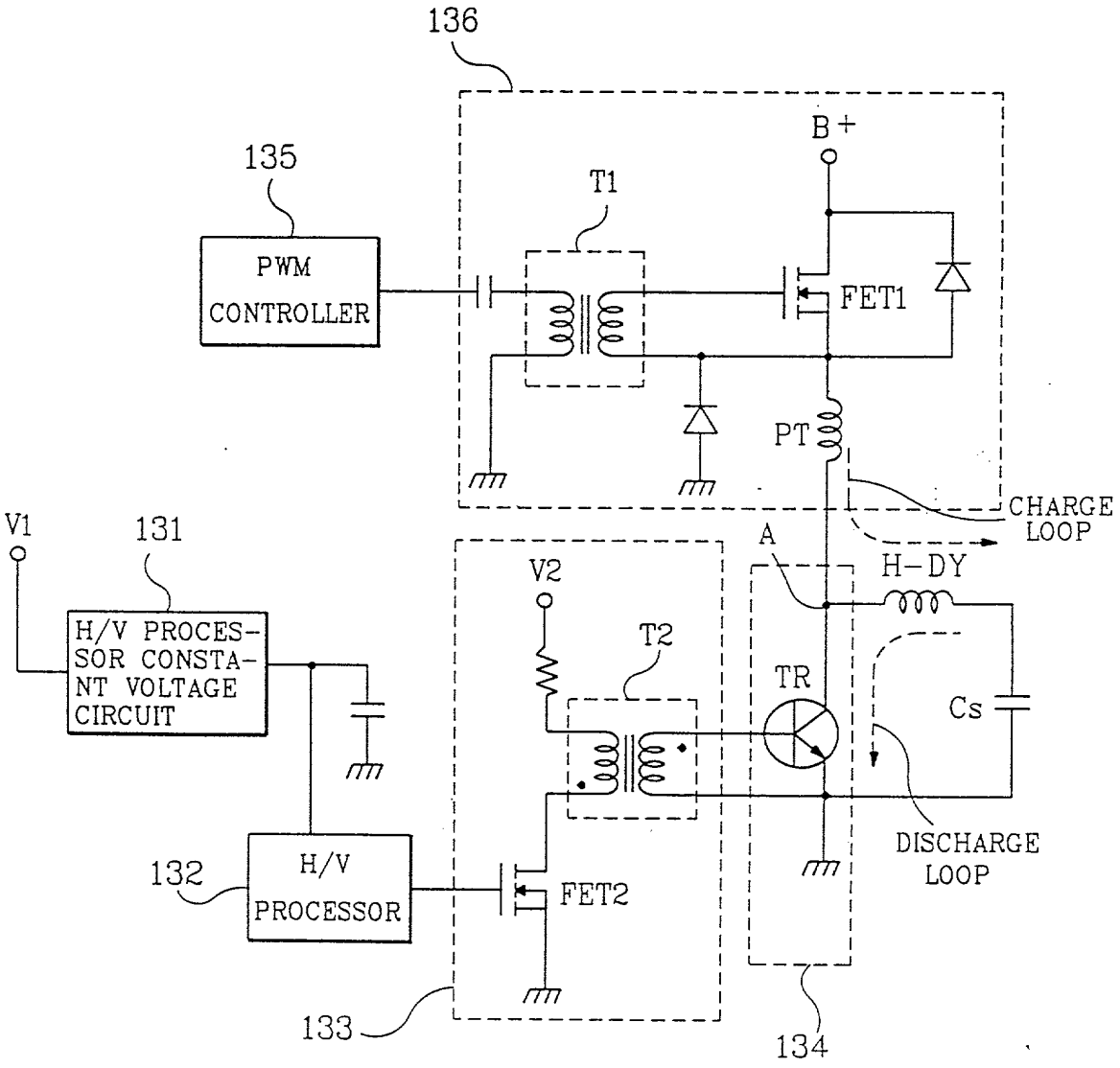

136
135
PWM CONTROLLER
T1
B+
FET1
PT
CHARGE LOOP
V1
131
H/V PROCESSOR CONSTANT VOLTAGE CIRCUIT
V2
T2
A
H-DY
TR
Cs
DISCHARGE LOOP
132
H/V PROCESSOR
FET2
133
134

FIG. 3

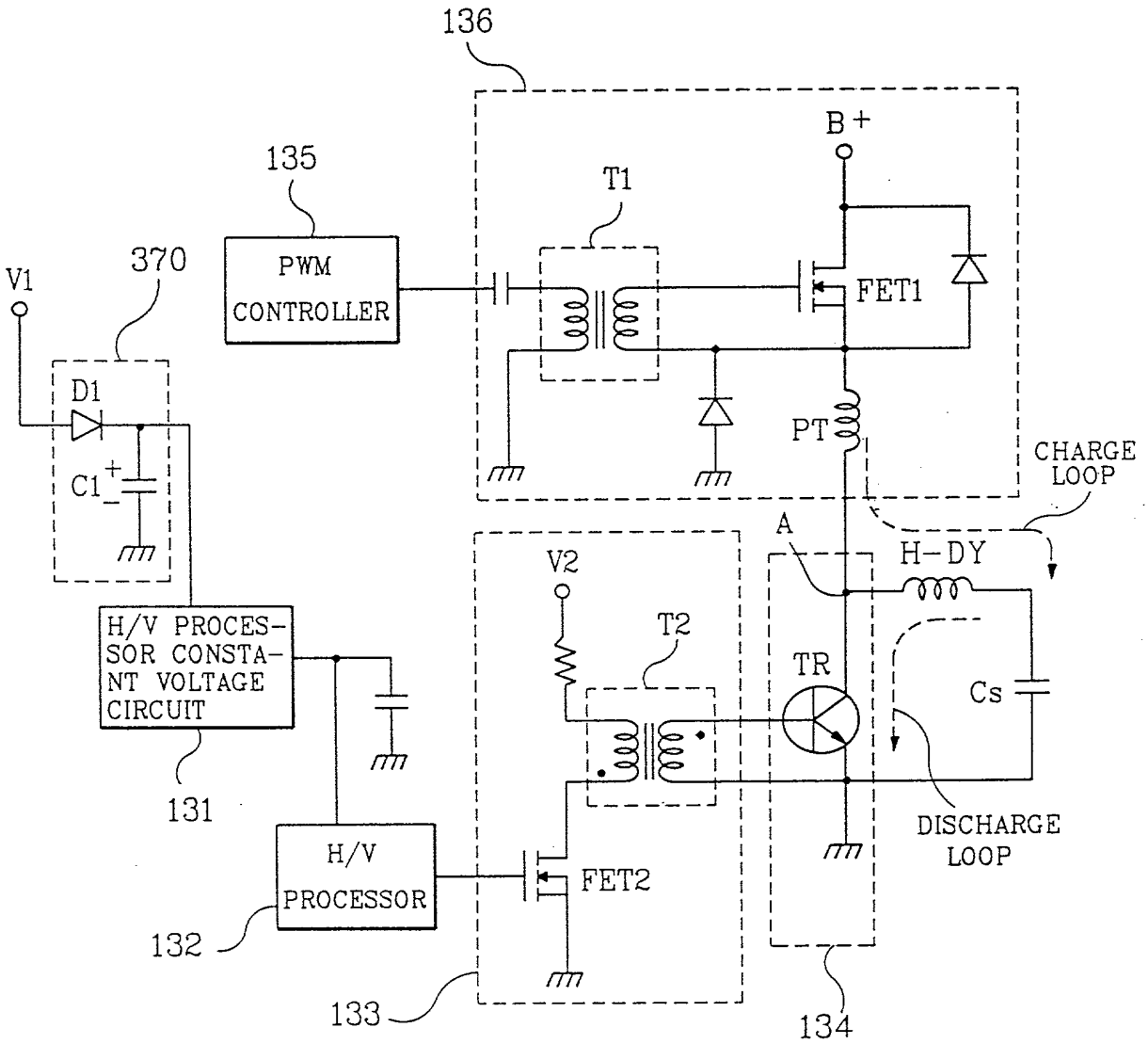

136
135
B+
T1
370
V1
PWM CONTROLLER
FET1
D1
C1
PT
CHARGE LOOP
A
H-DY
V2
T2
H/V PROCESSOR CONSTANT VOLTAGE CIRCUIT
TR
Cs
131
DISCHARGE LOOP
H/V PROCESSOR
FET2
132
133
134

FIG. 4A

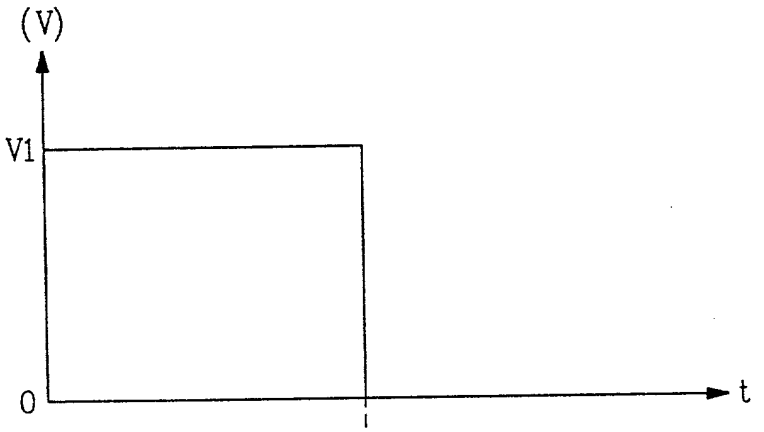

(V)
V1
0
t

FIG. 4B

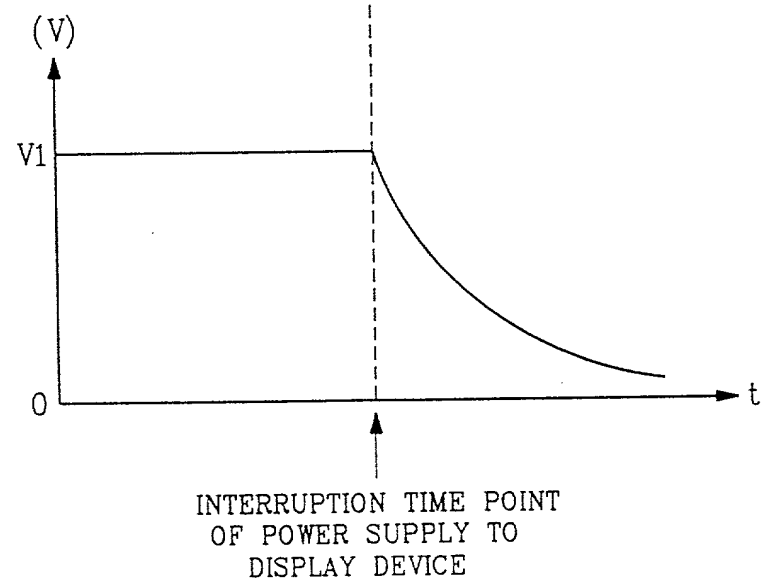

(V)
V1
0
t
INTERRUPTION TIME POINT
OF POWER SUPPLY TO
DISPLAY DEVICE

FIG. 5A

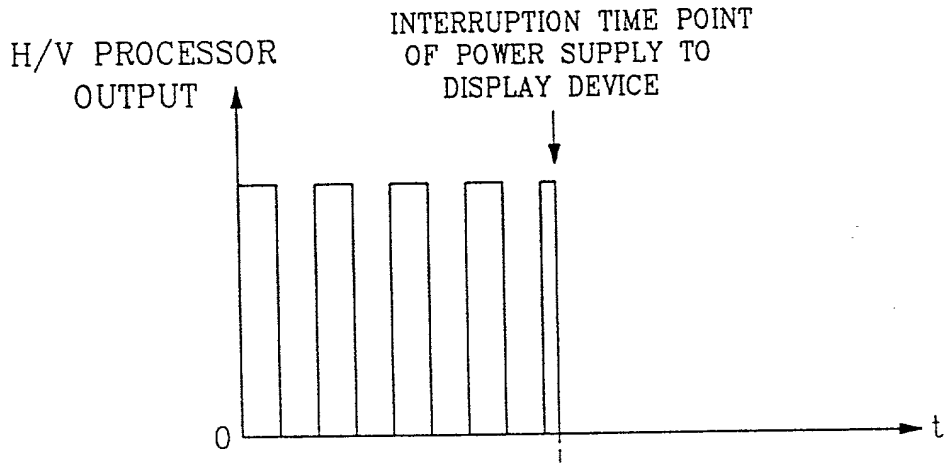
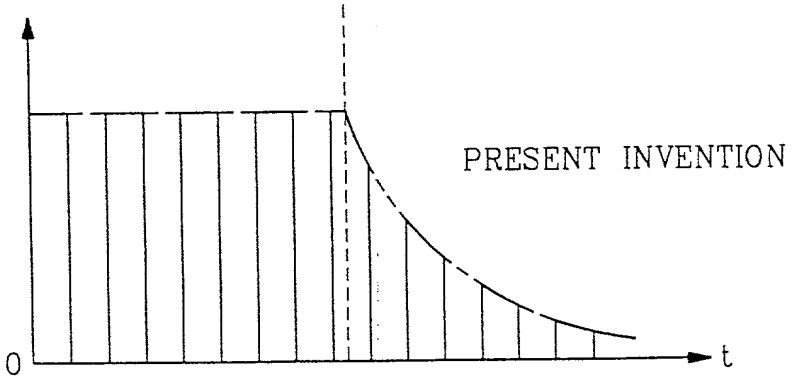

H/V PROCESSOR
OUTPUT
INTERRUPTION TIME POINT
OF POWER SUPPLY TO
DISPLAY DEVICE
0
t

FIG. 5B


PRESENT INVENTION
0
t

PATENT
P54766

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Geun-Woo PARK

Serial No.: *To be assigned* Examiner: *To be assigned*

Filed: 2 September 1997 Art Unit: *To be assigned*

For: DISPLAY DEVICE WITH POWER INTERRUPTION DELAY FUNCTION

TRANSMITTAL OF DECLARATION

The Assistant Commissioner
for Patents
Washington, DC 20231

Sir:

This transmittal accompanies an original Declaration for the above-referenced application.

Respectfully submitted,

Robert E. Bushnell,
Attorney for the Applicant
Registration No.: 27,774

Suite 425, 1511 "K" Street, N.W.
Washington, D.C. 20005
(202) 638-5740

Folio: P54766
Date: 09/02/97
I.D.: REB/kt

PTO/SB/01 (6/95)

DECLARATION

Docket No. P54766

AS A BELOW NAMED INVENTOR, I hereby declare that:
My residence, post office address and citizenship are as stated next to my name.
I believe that I am the original, first and sole (*if only one name is listed below*), or an original, first and joint inventor (*if plural names are listed below*), of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE: **DISPLAY DEVICE WITH POWER INTERRUPTION DELAY FUNCTION**

the specification of which either is attached hereto or otherwise accompanies this Declaration, or:

☐ was filed in the U.S. Patent & Trademark Office on _____ and assigned Serial No. _____.

☐ and (*if applicable*) was amended on _____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability and to the examination of this application in accordance with Title 37 of the Code of Federal Regulations §1.56. I hereby claim foreign priority benefits under Title 35, U.S. Code §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, or §119(e) of any United States provisional application(s), listed below and have also identified below any foreign applications for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

(Application Number)	(Country)	(Day/Month/Year filed)	Priority Claimed:
37143/1996	KOREA	30 August 1996	Yes [X] No [ ]
			Yes [ ] No [ ]
			Yes [ ] No [ ]

I hereby claim the benefit under Title 35, U.S. Code, §120, of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of Title 35, U.S. Code, §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, The Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(STATUS: patented, pending, abandoned)

I hereby revoke all previously granted powers of attorney and appoint the following attorneys: Robert E. Bushnell, Reg. No. 27,774, and Michael D. Parker, Reg. No. 34,973, to prosecute this application and to transact all business in the U.S. Patent & Trademark Office connected therewith and with any divisional, continuation, continuation-in-part, reissue or re-examination application, with full power of appointment and with full power to substitute an associate attorney or agent, and to receive all patents which may issue thereon, and request that all correspondence be addressed to:

Robert E. Bushnell,
Attorney-at-Law
Suite 425, 1511 "K" Street, N.W.
Washington, D.C. 20005-1401

Payor No. 008439
Area Code; 202-638-5740

I HEREBY DECLARE that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 U.S. Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF FIRST OR SOLE INVENTOR: GEUN-WOO PARK Citizenship: KOREA

Inventor's signature: Geun Woo Park Date: August 30, 1997.

Residence & Post Office Address: 472-21 Woonam1-dong, Paldal-gu, Suwon-city, Kyungki-do, Korea

FULL NAME OF SECOND JOINT INVENTOR: _____ Citizenship: _____

Inventor's signature: _____ Date: _____

Residence & Post Office Address:

FULL NAME OF THIRD JOINT INVENTOR: _____ Citizenship: _____

Inventor's signature: _____ Date: _____

Residence & Post Office Address:

FULL NAME OF FOURTH JOINT INVENTOR: _____ Citizenship: _____

Inventor's signature: _____ Date: _____